

## **Digital devices and technologies**

1 Properties of digital devices

2 Integrated digital devices

3 CMOS technology

4 Unused inputs of digital devices

5 Use of switches in logic circuits

6 Dynamic logic circuits

7 Three-state outputs and open collectors

7.1 Circuits with three-state outputs

7.2 Outputs with open collectors

7.3 Parallel grouping of three-state devices

7.4 Parallel grouping of devices with open collectors

7.5 Bus terminators

# Digital devices and technologies

## 1 Properties of digital devices

Digital devices process digital signals. For easy connection of devices in the network without the need for calculations and control of input and output voltages, the principle of **reserves** in the H and L levels between the output of one and the input of the next device is introduced. The voltage  $U_{OHmin} > U_{IHmin}$  is thus defined at the output, similarly  $U_{OLmax} < U_{ILmax}$ . As the signal passes through the device from input to output, the band gap **expands**. This is achieved by using an active element inside the part. However, it is not an amplifier in the usual sense, where linear circuits serve this purpose, while digital circuits are very nonlinear. The voltage levels are shown in the following figure 1.

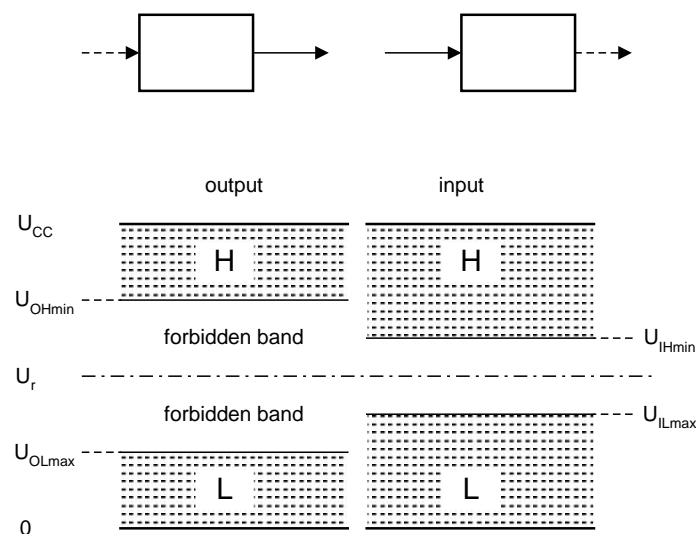


Fig. 1: Input and output voltage levels

**Voltage reserves** guarantee the operation of the circuits even at the extreme and most unfavorable values of temperature, supply voltage, output load, and superimposed interference. It should be remarked that some devices are based on the principle of (semiconductor) switches connecting the input to the output; the principle of voltage reserve is then not observed.

The dependence of the output voltage on the input voltage of a simple device - a "logic element" - is given by the **transfer characteristics**. Fig. 2 on the left shows the characteristics and the component which does not negate the input signal, in the middle the characteristic of the component is negative, in the right the characteristics and with **hysteresis** (non- negative ).

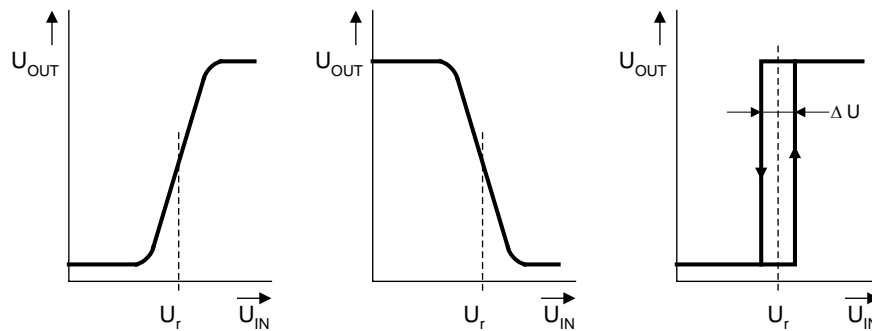


Fig. 2: Typical transfer characteristics of logic devices

In the narrow region just around  $U_r$ , the device acts as an amplifier with a gain of several hundred. If the input signal **changes slowly** and passes through this area for a long time, the part may **oscillate**. The word "long" is relative and here means a few units  $t_{pd}$ . That is why the "quality" of the signal is so important, which means sufficiently steep edges ( $dU/dt$ ). If this cannot be guaranteed, a device with a hysteresis characteristic must be used. Hysteresis is caused by internal positive **feedback**. The effect of a slowly changing signal on a device without hysteresis can be seen in Fig. 3 on the left, the effect on the device with hysteresis in the picture on the right. The **slow** passage through the reference level and even repeated transitions in the range of  $\Delta U$  do not matter.

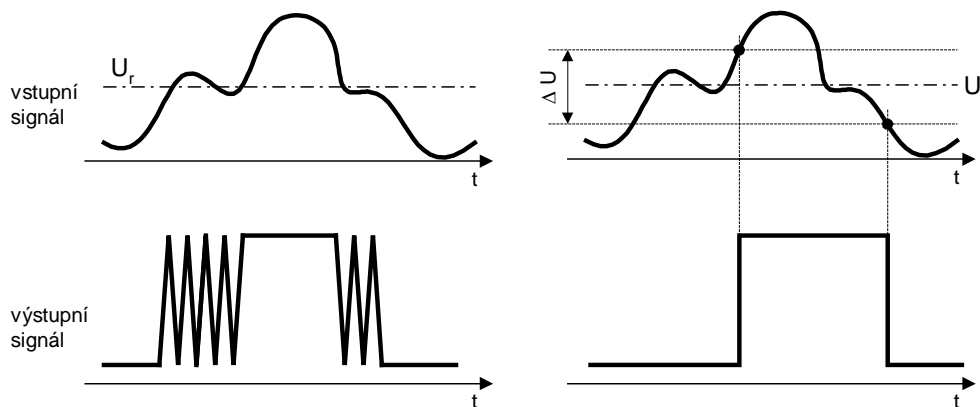


Fig. 3: Behavior of a device without hysteresis and with hysteresis in case of slowly changing signal

The output of a digital device is always loaded either by the inputs of following devices, or by a load of another character. We will call the second case a **non-standard load**. A non-standard load can be, for example, a resistor and an LED.

The load of the component changes the output voltage levels as well as the dynamic parameters of the signal. At present, the digital components are produced almost entirely in unipolar technology (CMOS) and, therefore, represent mostly a purely capacitive load. The parasitic capacities of the connections also contribute to this. The capacitive load does not affect the steady state voltage, but worsens the **waveform** of the signal, especially the parameters  $t_{pLH}$  and  $t_{pHL}$ . In this case, the output load is limited so that the system meets the requirements for speed.

In the case of non-standard loads, the output characteristics of the device may be important - see Fig. 4. The figure on the left shows the case of output current load in state H, the figure on

the right shows the case of current load in state L. It is obvious that the output voltage gets out of permissible range. This may not damage the component itself, but such a signal can no longer be used for other parts of the digital system.

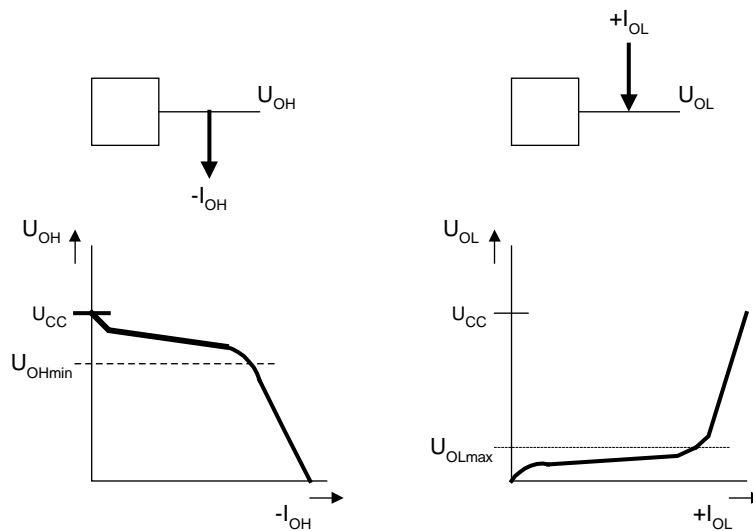


Fig. 4: Dependence of output voltage on output current

## 2 Integrated digital devices

Digital devices are manufactured exclusively in an integrated version, but with varying degrees of integration. As a small integration, **SSI** (tens to hundreds of transistors on chip), are referred to as "**gates**", which are basic digital components in the design of digital systems. The most common gates are shown in Fig. 5.

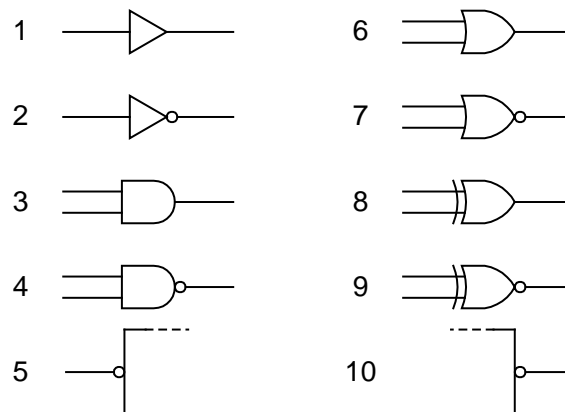


Fig..5: Schematic symbols of elementary logical members

The meaning of the individual symbols is given in the following table. Y is assumed as the output signal, A and B as input signals. The signal repeater (1) does not perform any logic function, but usually supplies higher output currents.

Tab. 1: Functions of elementary logical members

symbol	importance	logical function
1	signal repeater	$Y = A$
2	inverter (NOT circuit)	$Y = \overline{A}$
3	logical product (AND)	$Y = A \cdot B$
4	negated logical product (NAND)	$Y = \overline{A \cdot B}$
5	negation at the input	
6	logical sum (OR)	$Y = A + B$
7	negated logical sum (NOR)	$Y = \overline{A + B}$
8	exclusive sum (EX-OR or also XOR)	$Y = A \oplus B$
9	negated exclusive sum (XNOR)	$Y = \overline{A \oplus B}$
10	negation at the output	

Medium scale integration circuits - **MSI** - contain hundreds to thousands of transistors, and implement complex functions such as decoders, multiplexers, flip-flops, counters, etc. (see other chapters).

Large scale integration circuits - **LSI** - or Very large scale integration - **VLSI** - contain millions to billions of transistors on a chip, which is sufficient to constitute the entire systems on a chip with very complex functions, a description of which needs thousands of pages in the manual.

Elementary circuits - gates - and possibly also circuits of medium integration, are used in the design of larger circuits as the smallest design unit. This applies to logical design as well as chip design.

Regardless of the degree of integration, **three internal stages** can be distinguished for each digital device. The input stage contains **protection circuits** to prevent damage to the component by static charges and provides a distinction between L and H levels, the second stage is used to **process** information, and the third stage contains **output circuits** providing the correct L and H output levels as well as the appropriate output currents. The intermediate stage can be very simple (eg in basic logic gates), but also very complex (e.g. for a microprocessor). The input and output stage for a given technology is essentially independent of the complexity of the component. With LSI and VLSI integrated circuits, it is quite common for the individual internal stages to have **different supply voltages**. It is always higher in the input stage and especially in the output stage, and it is lower in the middle stage. This is because most circuits are concentrated there, where speed and power saving are essential. Modern technologies achieve this while constantly reducing the supply voltage. On the contrary, the output circuits must supply the necessary current for fast charging and discharging of load capacities and their supply voltage is usually higher. Separate power supplies (even ground connections) are necessary for limiting the **mutual interference** of internal circuits.

Manufacturers usually do not provide an internal circuit diagram (except for elementary gates), but always provide **equivalent** input and output circuit diagrams. The operation of complex internal circuits is then described in a manner typical of the device type - for example, by an instruction set for a microcomputer.

### 3 CMOS technology

Digital circuits are currently manufactured exclusively in **CMOS** technology (Complementary MOS). It is a combination of MOS transistors with N and P channels.

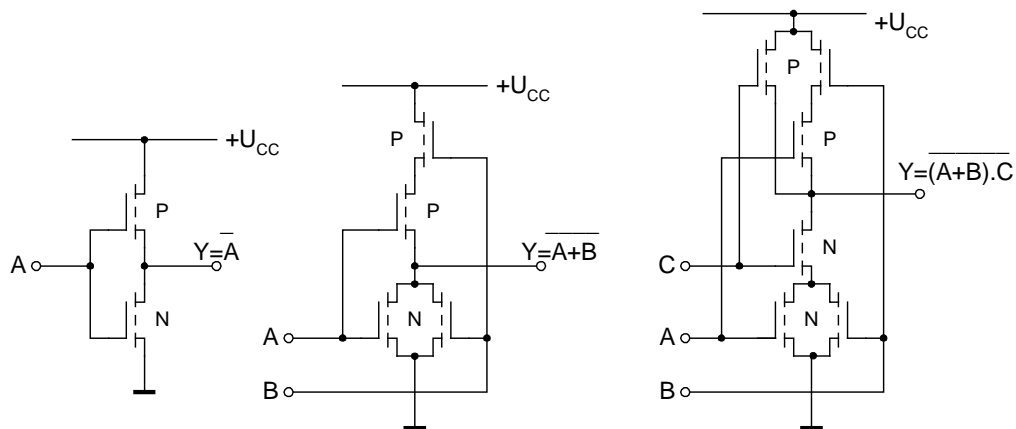


Fig. 6: Basic connections (gates) in CMOS technology

The inverter is shown in Fig. 6 on the left, the NOR gate in the middle and the device performing the function  $\overline{(A+B)} \cdot C$  on the right.

In the case of an inverter, the level H at input A opens the channel of the NMOS transistor, but at the same time the channel of the transistor PMOS is closed (there is only a small or zero voltage between its G and channel P). The opposite is true at the L level at the input - the NMOS transistor does not conduct and the PMOS transistor does. Both transistors thus alternate in the opening and closing of the channels and in the steady state, one of them is always non-conductive. Therefore, no current flows from the power supply (exactly - only a very small current of the order of nA ).

A similar principle of alternating the conductivity of the upper branch and the lower branch (i.e. PMOS and NMOS transistors) is used in more complex circuits. The figure in the middle shows the NOR gate. The parallel connection of NMOS transistors in the lower branch implements NOR function - any input in the state H opens at least one transistor and the output is then connected to ground, i.e. in the state L. Conversely, a series connection of PMOS transistors in the upper branch behaves in opposite way - in the state H on any input, at least one transistor (PMOS) is closed and the whole group does not conduct current from the power supply. With all inputs at L, the upper branch conducts and the lower branch does not. Therefore, the output is state H - again, no current flows from the power source.

It is obvious that the **series** connection of the transistors corresponds to the **logical product** (AND), and a **parallel** connection corresponds to a **logical sum** (OR).

More complex circuits can be designed using the fact that the logic expression describing the connection of the upper branch must always be **dual** to the logic expression describing connection of the lower branch. Simply, the logic sum is exchanged for the logic product and vice versa.

The picture on the right shows the circuit that implements the function  $Y = \overline{(A + B) \cdot C}$ . This corresponds to the lower branch, where the sum of  $A+B$  is realized by a group of two transistors connected in parallel and also the product of the variable  $C$  as a transistor in series with this group. The upper branch is connected in exactly the opposite way, i.e. as  $(A \cdot B) + C$ . This guarantees that the conductivity of the two branches alternates.

During transients, when the input voltage is around half the supply voltage, both branches are partially open and the circuit draws an increased supply current. The length of this situation depends on the transients time  $t_{pLH}$  and  $t_{pHL}$ . This results in current pulses in the power supply distribution and thus an increase in the power consumption of the device, proportional to the frequency of switching between the L and H states. This is particularly pronounced for signals with **slow transients**. The dependence of the supply current  $I_{CC}$  on the input voltage  $U_i$ , i.e. the **consumption characteristics**, is shown in Figure 7.

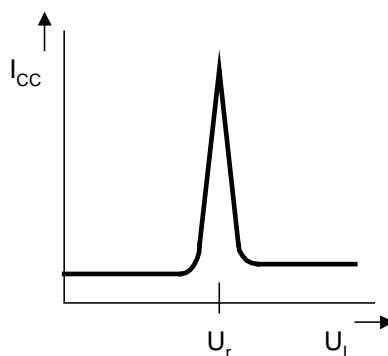


Fig. 7: Inverter consumption characteristic

The processing of logical variables is a matter of the intermediate stage of the device. The first stage of CMOS devices always contains **voltage limiters** on the signal inputs according to Figure 8.

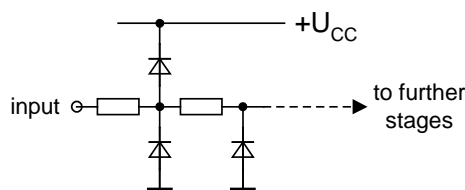


Fig.8: CMOS input voltage limiter

The input circuit protects other internal circuits mainly from the consequences of **static charge** applied to the input. Due to the very high input resistance of MOS transistors (of the order of  $10^{12} \Omega$ ), even a very small charge can cause a breakdown of an oxide under the gate and destroy the circuit. It should be remarked that the path for positive charges (via  $+U_{CC}$ ) only exists for a device installed in the system - there is a much greater risk of damage if the component is not yet connected.

The output stage of the CMOS component is equipped with transistors with low channel resistance (wide and short channel), capable of supplying a large output current.

Another reason for unwanted increase of the power consumption is the influence of the **parasitic capacitances** existing inside the integrated circuit and at its outputs. When the state changes from L to H, the capacitor with capacitance  $C_p$  is charged by a voltage jump  $\Delta U$ . Subsequently, when changing from H to L, it is discharged with the same jump. This consumed the charge  $Q_{pp}$  from the power supply. The same charge would correspond to a constant current  $I_{CC}$ , flowing for  $\Delta t$  time. We can write

$$Q_p = C_p \cdot \Delta U = I_{CC} \cdot \Delta t, \text{ and so}$$

$$I_{CC} = C_p \cdot \frac{\Delta U}{\Delta t} = C_p \cdot \Delta U \cdot f,$$

where  $f$  is the switching frequency for oscillations between the L and H states, or the **operating frequency**. To calculate the power input from the power supply, it is necessary to know the magnitude of the voltage jump  $\Delta U$ . Assume that the voltage drops on open transistors in Fig. 6 are negligible, and therefore  $\Delta U = U_{CC}$ . Then the power increase due to parasitic capacitances is

$$P_p = U_{CC} \cdot I_{CC} = C_p \cdot U_{CC}^2 \cdot f$$

The result is an approximately **linearly increasing** power consumption of CMOS devices with an operating frequency. This is also the reason why the power consumption of CMOS devices is usually stated in  $\mu\text{W}/\text{kHz}$ . At other times, the power input in the static state (i.e. with zero operating frequency) and the power input at a defined operating frequency are stated. Static power is low in CMOS circuits. From the above relationship, it is also clear the importance of reducing the **supply voltage**, which here occurs in a **square**. Reducing parasitic capacities is also significant. Increasing the integration density and the associated reduction in the size of the transistors results in a reduction in capacitance and supply voltage.

The power dependence of CMOS circuits as a function of frequency is shown in the following Figure 9. The power scale shows no values - it depends on the complexity of the circuit. The characteristic clearly shows the influence of a steady-state current due to residual currents of junctions and insulators. With increasing integration density, these additional power components are becoming increasingly important.

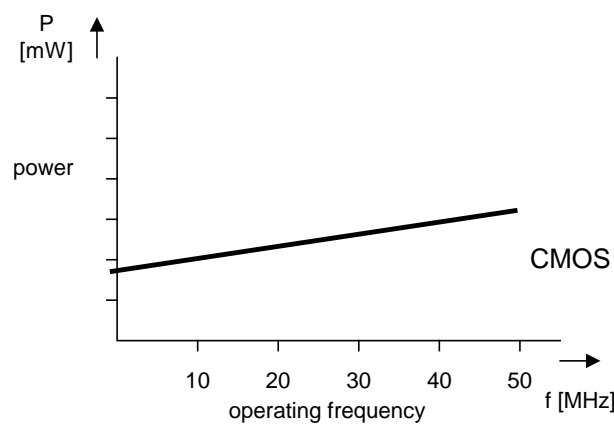


Fig. 9: Dependence of input power on operating frequency



As the result of the development of CMOS circuits, the transistors shrunk and connections shortened. At the same time the supply voltage gradually reduced from 5V over 3.3V, 2.5V, 2V, 1.8V, 1.5V, 1.2V, 1V, 0.8V, and this trend will certainly be continued in future. Reducing the dimensions means smaller parasitic capacitances and shorter delays in connections, reduced supply voltage means smaller voltage jumps - all this contributes to the acceleration of the circuits and, at the same time, to reducing their power consumption.

In the context of small and medium integration, several variations of "**logic families**" have been developed, each with the same logic functions, but different electrical parameters (speed, consumption, supply voltage). In CMOS technologies, these were typically the **HC**, **AHC**, **AC** series with a 5V power supply, or **LVC**, **ALVC** with a 3.3 V power supply, and many others. The delay  $t_{pd}$  of these circuits ranges around several nanoseconds.

The **4000** and 4500 series have exceptional properties for use in demanding conditions of increased **interference**. The circuits are deliberately **slow** (  $t_{pd}$  around 100 ns ), which is favorable for interference suppression. They allow supply voltages from 3 to 15 V, which means very small demands on the stability of the supply voltage. At higher supply voltages, the circuit has greater margins between L and H levels and thus greater immunity to interference.

However, the domain of CMOS circuits is in the VLSI circuits, such as memories, microprocessors, and single-chip microcomputers. Small and medium integration circuits are used for additional functions - so called "**glue logic**" - and support of the high integration circuits.

The voltage levels of CMOS circuits may or may not be **compatible** with each other. Compatible circuits can and incompatible circuits cannot work together. Compatibility is guaranteed, for example, for some circuits with a 5 V supply and some with a 3.3 V supply voltage.

#### 4 Unused inputs of digital devices

Unused inputs are common. For **CMOS** circuits, leaving an unconnected input is completely out of the question. The input impedance of these circuits is very high and the unconnected input thus can be disturbed by parasitic connections to external or internal circuits. Furthermore, if the voltage at the unconnected input approaches the reference level, the **supply current** will increase. Figure 10 shows methods of treating unconnected inputs.

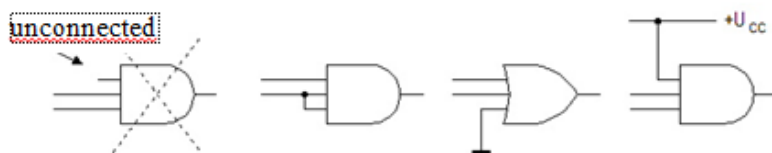


Fig. 10: Treatment of unused inputs

## 5 Use of switches in logic circuits

Logic circuits with switches - "**Pass Transistor Logic**" (PTL) - are advantageous for some functions. Symbolically shown switch controlled by logic signal  $A$  is shown in Fig. 11 a) . It is assumed that the switch is "ON" at the control signal in state '1' and the switch is "OFF" at the control signal in state '0'. The principle of a real switch with an NMOS transistor is shown in Fig. 11 b). Switching ON requires applying a voltage between the gate and the channel greater than  $U_T$  (threshold voltage). The open channel has a resistance  $R_{ON}$  of the order of several hundred  $\Omega$ . Switching OFF requires applying a voltage between the gate and the channel smaller than  $U_T$ . The closed channel has a resistance  $R_{OFF}$  of the order over  $10^9 \Omega$ . However, this means that the control signal  $A$  must have a higher level  $U_H$  than the switched signal ( $X$ ,  $Y$ ). This is very impractical - it would require the distribution of additional (higher) supply voltage, special generation and distribution of control signals, etc.

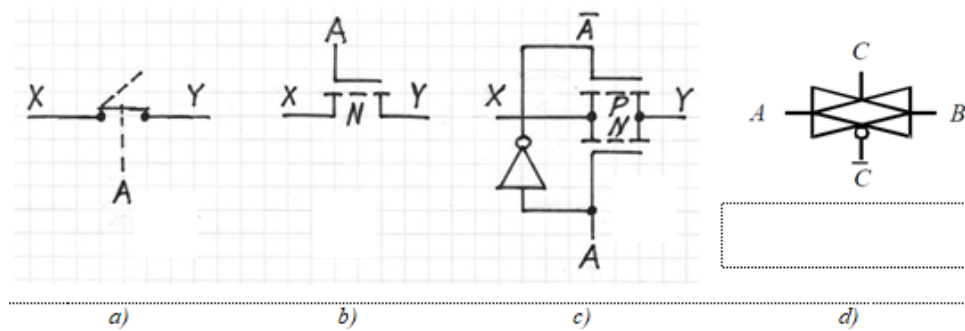


Fig. 11: a) symbol, b) NMOS switch, c) CMOS switch, d) CMOS switch symbol

These shortcomings are fully eliminated by a **complementary** switch with NMOS and PMOS transistors - the CMOS switch, depicted in Fig. 11 c) . For closing the switch,  $A = 1$  and  $\bar{A} = 0$ , and thus the voltage at the gate of the NMOS is  $U_H$  and  $U_L$  is at PMOS. When the signal  $X$  is  $U_L$ , the NMOS has a positive gate voltage  $U_H - U_L$  against the channel and will be ON; at the PMOS gate there is only a very low voltage with respect to the P channel and hence the PMOS is OFF. Conversely, with the  $X$  signal at  $U_H$ , the NMOS will have only a very low voltage relative to the N channel and will be turned OFF; there will be a negative voltage  $U_L - U_H$  on the PMOS gate and this transistor will be ON. If the voltage difference  $|U_H - U_L| > |U_T|$ , one of the two transistors will always be ON regardless of the state of the  $X$  signal. With the control signal  $A = 0$  and  $\bar{A} = 1$ , both transistors will be OFF. As a result, the CMOS switch provides connection between the points  $X$  and  $Y$  without increased demands on the control signal.

CMOS switches are well used in both analog and digital circuits. Here, however, we will only deal with applications in digital circuits. Certain rules can be observed in all connections - see Fig. 12 with symbolic switches. In case 12 a) the intention was to disconnect the  $X$  signal from the input of the AND gate - however, in CMOS technology, the input resistance of the logic component is of the order of  $10^{12} \Omega$  and more, while the  $R_{OFF}$  of the switch is of the order of  $10^9 \Omega$ . Therefore, the circuit would never be disconnected. This connection **cannot be used**.

Fig. 12 b) shows a circuit with two switches which connect either the signal  $X$  or the signal  $Y$  to the input of the AND gate. This connection works reliably, because one switch is always ON and thus the signal  $W$  is defined. Conditions at the point  $W$  are given by  $A.X + \bar{A}.Y$  and the circuit realizes the function of a **multiplexer**.

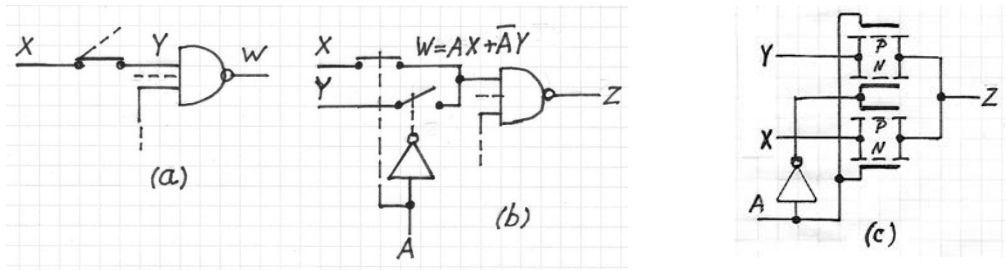


Fig. 12: Switches at the logic gate inputs

- a) single switch at the input
- b) alternating switches
- c) multiplexer with switches

Fig. 13 shows a four-channel multiplexer (signal switch), again with symbols in place of the switches. The switches are controlled in such a way that **just one** is ON **at a time**.

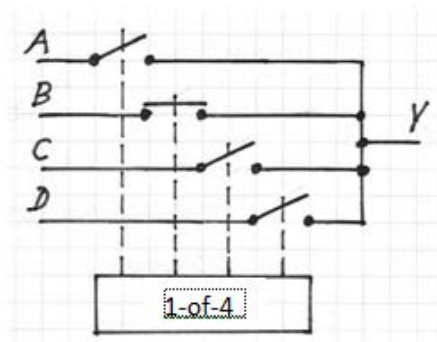


Fig. 13: Four-channel multiplexer with switches

The switches can be advantageously used for the implementation of some logic functions. The following pictures show two of them. This time, the switches are drawn with transistors according to reality, so that the simplicity of this implementation is obvious.

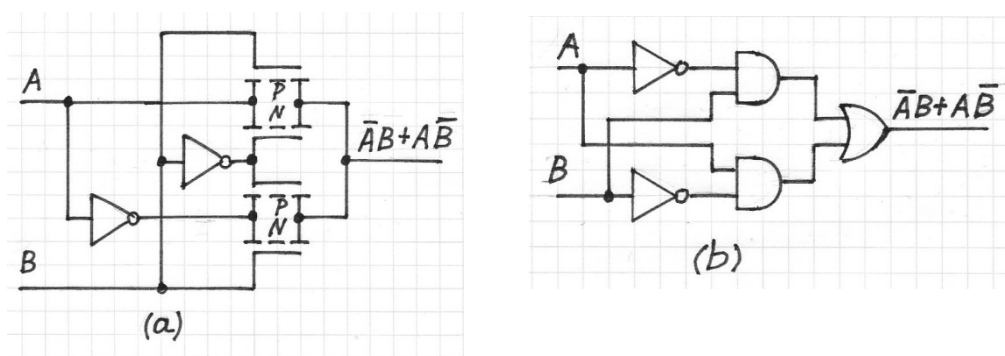


Fig. 14: Non-equivalence circuit, EX-OR

- a) with switches
- b) with gates

The **EX-OR** circuit, also called XOR, has a very wide use as a function of "**non-equivalence**", or an odd parity generator, also **modulo 2**, and is part of a number of circuits. Its function can be written as  $\bar{A} \cdot B + A \cdot \bar{B}$  or with a special symbol as  $A \oplus B$ . The circuit

gives a value of '1' for **mismatched** inputs. The simplicity of implementation with switches, as compared to gates, is obvious.

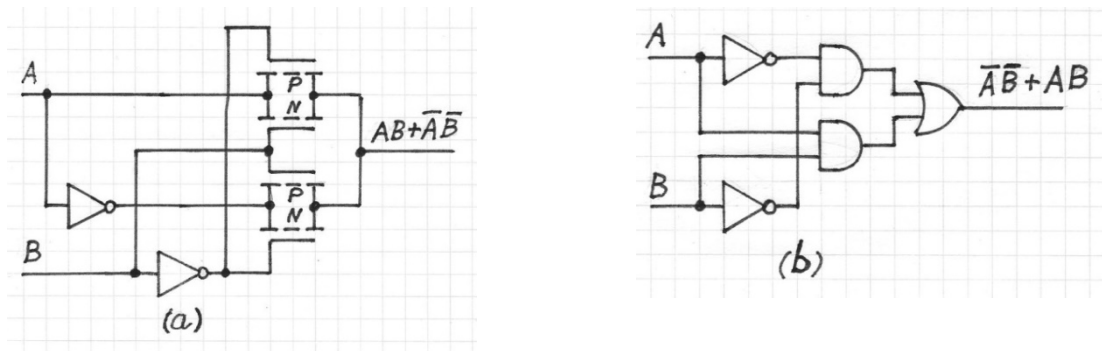


Fig. 15: Equivalence circuit  
a) with switches  
b) with gates

The **equivalence** circuit, also called XNOR, gives the value '1' for identical inputs. Its function can be written as  $\bar{A}.B + A.\bar{B}$  or with a special symbol as  $A \equiv B$ . Again, the simplicity of implementation with switches is obvious.

## 6 Dynamic logic circuits

According to the behavior in time, logic circuits can be divided into static and dynamic circuits. For **static** circuits, the output signal is constant and valid for as long as the input signals are constant. For **dynamic** circuits, the output signal is only valid for a limited time, even with constant input signals. Obviously, the charge on the capacitor is substantial here.

The principle of the dynamic circuit is shown in Fig. 16.

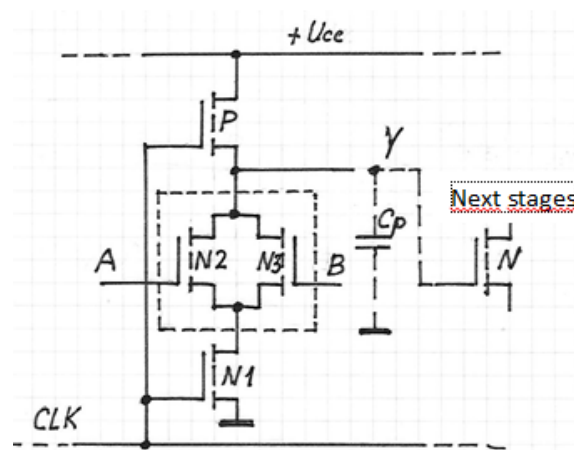


Fig. 16: Principle of dynamic logic circuits (here NOR)

**Synchronization pulses** (clock pulses, CLK) control the charging of capacitor  $C_p$ . When  $CLK=0$ , transistor P is switched on and N1 is switched OFF. This charges  $C_p$  to the value of the supply voltage  $+U_{CC}$ . When N1 is switched OFF, the current path through N2 and N3 is

blocked. This phase of the operation is called a "**precharge**". When  $CLK = 1$ , P is switched OFF and N1 is switched ON. This opens the way for the current discharging  $C_p$ . However, it also depends on the state of transistors N2 and N3, which realize a logical function of variables  $A$  and  $B$ ; in this case it is a NOR function. Accordingly,  $C_p$  either discharges or remains charged. This phase of operation is called as "**evaluation**". The logic function is created by the functional circuits, i.e. by the connection inside the dashed rectangle. Naturally, the function may be different from that shown in Fig. 16. The output  $Y$  can be sent to other stages and thus the whole combinational circuit can be formed. It should be noted that the logic function is valid only during the evaluation phase, while during the precharging phase  $Y$  changes and ends by  $Y = U_{CC}$ .

Compared to static CMOS logic, the advantage of dynamic circuits is a **smaller number** of transistors and thus a smaller area on the chip - the NOR circuit in CMOS logic would have  $2n$  transistors at  $n$  inputs, but only  $n + 2$  in dynamic logic. With a more complex function, the difference is noticeable. Another advantage is higher speed (up to  $2x$ ).

There are also disadvantages and problems. During the evaluation phase, the **unwanted** (false) pulse 0-1-0 must not occur on the inputs even for a short time. This could cause discharging the capacitor and a false state '0' would appear at the output till the next precharging phase.

During the evaluation phase, the capacitor will either discharge or remain charged. In this case, the unwanted discharge by the reverse currents of the PN junctions and the currents on the chip surface can happen. If this phase lasts too long, the voltage may drop below the minimum  $U_H$ . Hence, the **minimum frequency** of the clock pulses is defined in dynamic circuits. There are also connections with a low-current auxiliary power source that constantly charges the capacitor. This can help to lower the minimum clock frequency.

Another problem occurs when two dynamic circuits are connected **in series**. The waveforms of the signals in the circuit according to Fig. 16 are shown in Fig. 17. Due to the small delay in the PMOS transistor, the charging of the capacitor is somewhat delayed by the time  $t_1$  behind the trailing edge of  $CLK$ . With the leading edge of  $CLK$ , PMOS turns OFF and transistor N1 and possibly N2 and N3 turn ON. This creates a path for possible discharge of the capacitor (in Fig. 17 with regard to variables  $A, B$ ) - the discharge is delayed by time  $t_2$ . Waveform 1 applies to the case that due to the implemented logic function and the state of the input variables a discharge occurs, course 2 applies to the case that no discharge occurs. During this time, the output  $y$  and the other inputs of the next circuit will be at state '1'. This will **discharge** the currently charged capacitor which will remain discharged during the evaluation phase - even if after time  $t_2$  the output  $y$  will reach state '0'. Therefore, the dynamic circuits of Fig. 16 **cannot be connected** in a cascade.

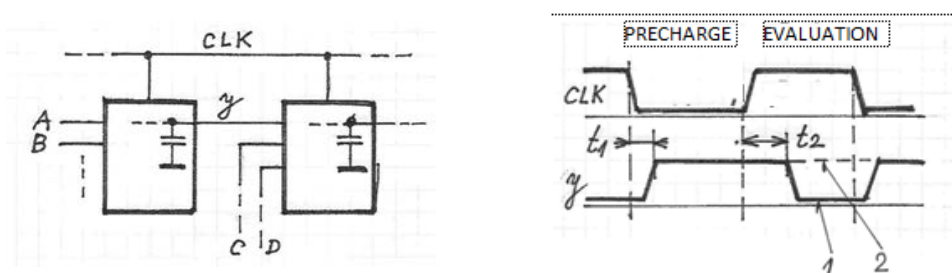


Fig. 17: Problematic connection of dynamic circuits

Correction is possible by introducing synchronization pulses into the subsequent stage **time-delayed** by a value of  $t_2$  (or more).

There is another way, so-called **domino logic** - see Fig. 18. There is always one static CMOS inverter between the two dynamic circuits and its output is opposite to the output of the first dynamic circuit. Therefore, a signal in state '0' is fed to the next dynamic circuit at the beginning of the evaluation phase, which **cannot** turn ON the NMOS transistors and thus discharge the memory capacitor - see the detail in the ring. Only later does state '1' appear (or '0' remains) and the capacitor discharges - compare with Fig. 17. Domino logic thus solves the problem of unreliable operation of a cascade of dynamic circuits. Dynamic logic is used in complex digital systems, such as microprocessors.

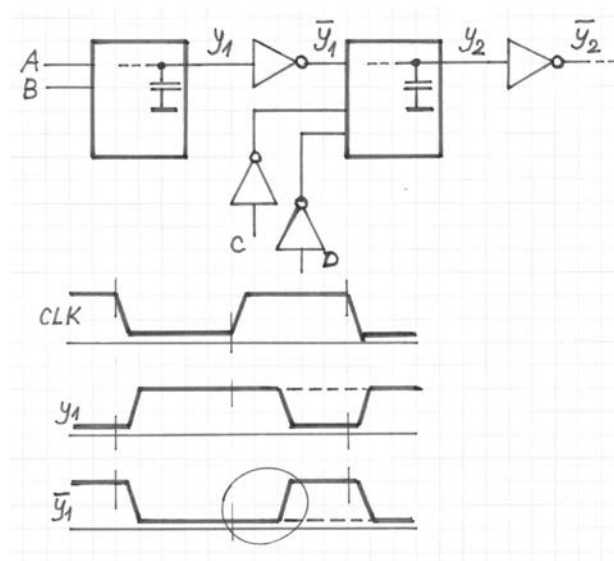


Fig. 18: DOMINO logic

## 7 Three-state outputs and open collectors

### 7.1 Circuits with three-state outputs

The three-state output circuit allows both transistors to be switched OFF. The output is then in a **high impedance** state (denoted by 'Z') and manifests itself only as a small **capacitor** (a few pF). The currents through closed transistors can be neglected. The signal generated by such a circuit can therefore take three values - '0', '1', 'Z'. The principle of output stage control in CMOS technology is shown in Figure 19.

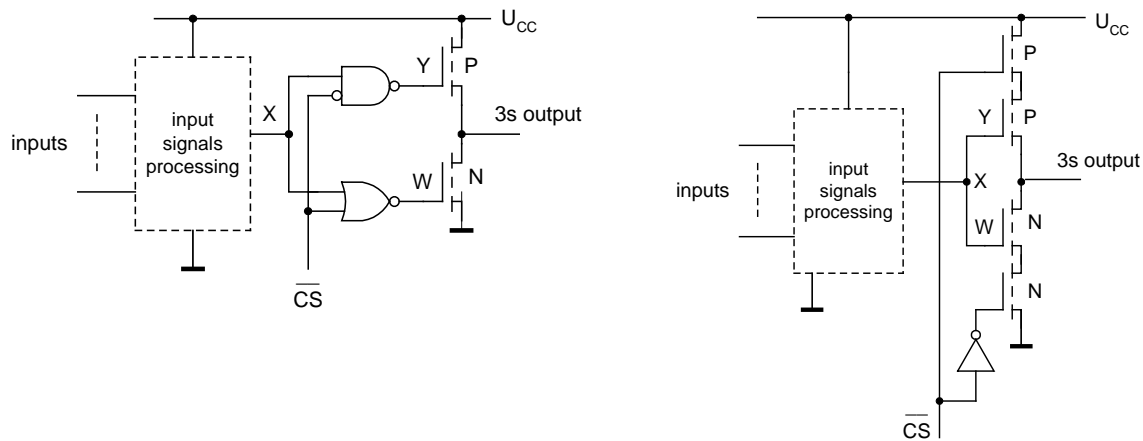


Fig. 19: Output circuit of a three-state device

The input of the selection signal  $\overline{CS}$  - **Chip Select** - controls the blocking or unblocking of the output. In the figure on the left it is evident that when  $\overline{CS}=1$ , then  $W = '0'$  and  $Y = '1'$ , and both transistors are turned OFF. Conversely, when  $\overline{CS}=0$ , then  $W = Z = \overline{X}$ , and the output will be equal to  $X$  (the output stage with NMOS and PMOS transistors negates). In the figure on the right, the 'Z' state is reached by a pair of transistors in series with the original inverter.

From the point of view of dynamic parameters, two signal paths are distinguished for three-state gates - on the one hand the path from input ( $X$ ) to output ( $Y$ ) with unlocked output ( $\overline{CS}=0$ ), on the other hand the path of control of high impedance state from input  $\overline{CS}$  to output. In the first case, the dynamic parameters do not differ from the parameters of common gates, so  $t_{pLH}$ ,  $t_{pHL}$  will be reported. In the second case, it is the **unblocking time**  $t_{pZY}$  and the **blocking time**  $t_{pYZ}$ . Fig. 20 shows the tri-state output signal, which is blocked for some time. The 'Z' state is usually indicated by dashed lines approximately in the middle of the amplitude as an expression of an undetermined output voltage. Blocking and unlocking times depend on the technology and range around a few ns.

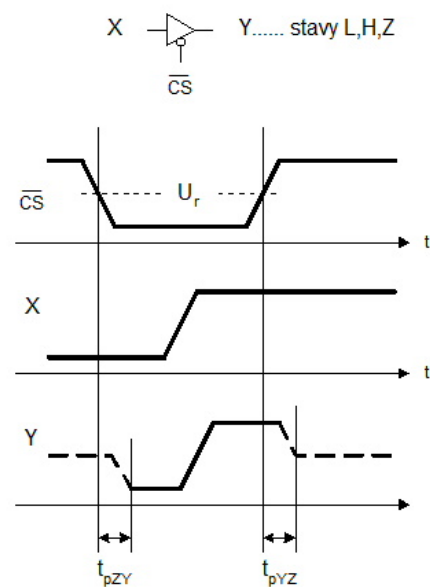


Fig. 20: Blocking the output of the three-state gate

The figure shows the simplest three-state element - the **bus driver** (BD). The signal is not logically processed by it; the only purpose is to control the connection and disconnection of the output. Available are both positive and negative bus drivers. Bus drivers are always the most powerful circuits in a given technological family.

The outputs of three-state gates can be connected in parallel. However, it must be ensured that at most one output is unblocked at any one time - otherwise large currents could occur



between the outputs if they are in different states (one in H and the other in L). When all outputs are blocked, there is an unspecified voltage on them - usually, this is also undesirable.

Three-state outputs can be integrated in more complex medium scale and large scale integration circuits. However, large scale integration circuits are not designed for high output currents (only a few mA). In the case of their loading with large parasitic capacitances (tens and hundreds of pF), the system would slow down significantly. Therefore, LSI and VLSI circuits are often separated from other circuits (e.g. buses) by additional bus drivers. In some circuits, the three-state outputs are not present at all, so separate bus drivers must also be used to connect them to the bus.

Many circuits have bidirectional terminals - they can function as inputs or outputs. This is especially true for computer data circuits like memories. **Bidirectional** bus drivers are used to connect such circuits to the bus. Their connection is shown in Fig. 21. The *DIR* signal controls the direction of transmission, the signal  $\overline{CS}$  then evokes the high-impedance state. When  $DIR=0$ , the direction of transmission is  $X \rightarrow Y$ , when  $DIR=1$ , the direction is  $Y \rightarrow X$ . At  $\overline{CS}=1$ , both outputs are in the high impedance state.

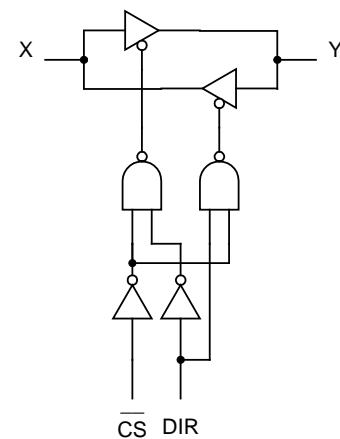


Fig. 21: Bidirectional bus driver

## 7.2 Outputs with open collectors

In this output circuit, there is only a transistor that grounds the output and thus ensures the L state - see Fig. 22.

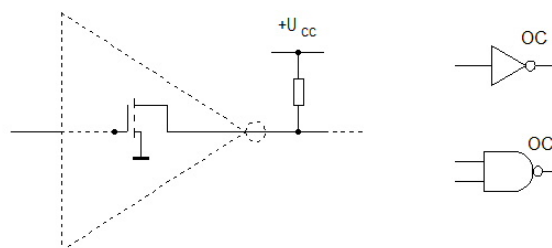


Fig. 22: Open collector output

The H state must be produced by an external resistor. Logic devices with open collectors exist both as inverters and as members implementing simple logic functions (NAND in Fig. 22). Their use results from the possibility of their **parallel connection**. However, the situation is different from that with three-state outputs. In the case of open collectors, it is not a problem if more than one of the devices connected in parallel has an L state at the output. The current is given by the value of a collector resistor, regardless of the number of transistors turned ON. The H state of the whole group occurs when all transistors are turned OFF. There is no risk of a collision here either.



### 7.3 Parallel grouping of three-state devices

The most common case of parallel connection of three-state devices is the **bus** - see Fig. 23. From an electrical point of view, it is a node. A bus is a wire or group of wires of the same nature (e.g. address or data bus) passing through the whole system to which individual circuits are connected.

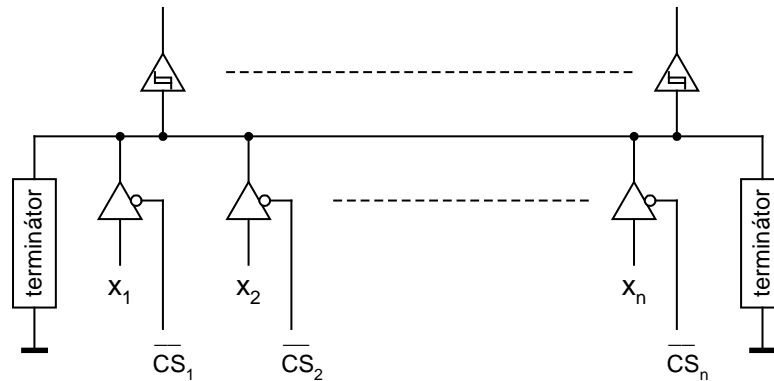


Fig. 23: Bus with three-state devices

Using the selection inputs ( $\overline{CS}$ ), one of the signals  $x_1, \dots, x_n$  can be selected and transmitted to any signal receiver via the bus. Inside the digital systems, like computers etc., signal is transmitted to the bus via the bus drivers. In communication over longer distances, there are specialized bus transmitters and receivers, very often joined together in **transceivers**. **Terminators** serve to limit the overshoot at the ends of the bus. In most cases, the bus must be regarded as an (electrically) long line. Overvoltage and ringing occurs at the line ends if the characteristic line impedance and the impedance at the line ends differ. Terminators therefore represent the appropriate impedance.

The bus is far from an ideal connection and it suffers from **interference** from other circuits in the system as well as effects caused by a non-ideal termination. Therefore, the receivers have a **hysteresis** characteristic that causes their reduced sensitivity to interference, overshoots, and slow transitions over the reference level. In high-speed circuits, it is necessary to take into account the effects of long lines in buses with a length of several cm.

### 7.4 Parallel grouping of open-collector devices

Open-collector devices are widely used for connection to a **bus**. Fig. 24 shows the connection of NAND gates (top) and inverters (bottom). The same principles apply to bus termination as in the case of three-state drivers. The resistors  $R_K$  take on the function of both collector resistors and terminators and are therefore placed at both ends of the bus.

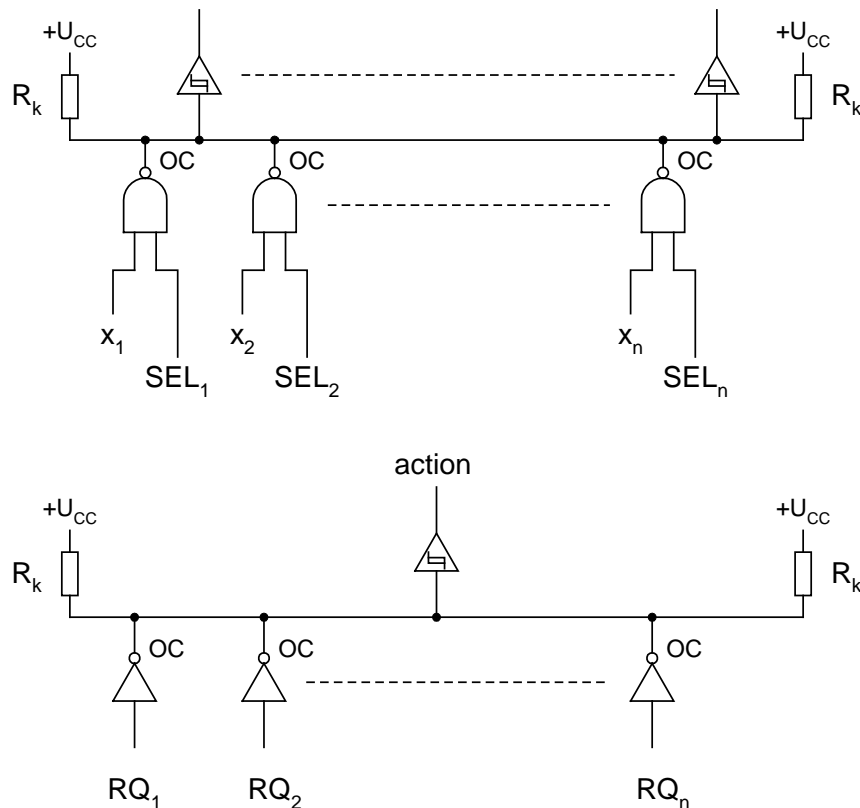


Fig. 24: Bus with open-collector devices

Both configurations have their application fields. The NAND gates on top can transmit their signal  $x_i$  (inverted) if their input  $SEL_i = 1$ . If more than one gate is selected, there will be no destructive event; only the transmitted data will be distorted. This situation is called "**non-destructive conflict**". The open-collector transmitters also exist in the power version for connection to fast serial buses, such as CANbus, with arbitration based on non-destructive conflicts.

The second, different application is shown at the bottom of Fig. 24. OC Inverters connected to the bus have no control input and therefore their only task is to force the L state on the bus if any signal  $RQ_i$  is active (i.e. in the H state). The whole arrangement is not intended for signals transmission, but for generation of a signal to start certain action if one or more requests exist. This is the case, for example, in computers, where program interrupts or resets and other actions are triggered in this way. Another example is the diagnostic system which, in case of one of many possible faults, triggers an action to prevent a dangerous condition.

The bus, to which the open collector circuits are connected, changes from state H to state L as fast as in the case of three-state gates - in both cases there is an open transistor on the way from the common bus to ground, through which the parasitic capacitances are quickly discharged. However, the transition from L to H is ensured only by an external resistor, the value of which cannot be too low. Therefore, the transition from the L to H state is **slower** - see Fig. 25. This must be taken into account when designing the system.

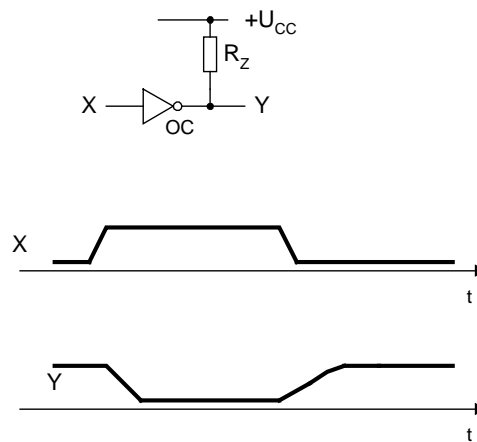


Fig. 25: Pulse rise deceleration for open collector circuits

### 7.5 Bus terminators

To prevent reflections, the line must be terminated with a resistor equal to the characteristic impedance of the line,  $Z_0$ ). A line implemented as a printed circuit typically has a  $Z_0$  close to  $100\ \Omega$ . The "start" and "end" of the line cannot be specified in case of the bus - transmitters and receivers can be connected anywhere. Therefore, it is necessary to use terminators at **both ends**. Each driver is thus loaded by a parallel combination of two terminators, which requires increased power. The effects of the long line and loaded drivers are particularly evident in large distributed systems, in which data is transferred serially over a common bus on the distance up to hundreds of meters.

The simplest terminators are shown in Fig. 26 on the left. For correct impedance termination of the bus,  $R_0 = Z_0$  must apply. The output current of the drivers is high in the H state and zero in the L state. The terminators in the figure on the right guarantee better current symmetry. The parallel combination of  $R_1$  with  $R_2$  is equal to  $R_0$  and the ratio of both resistors is such that with all exciters disconnected, the voltage on the bus acquires a required value (e.g. slightly above  $U_r$ . For example, for  $Z_0 = 100\ \Omega$ , a combination of  $R_1 = 180\ \Omega$  and  $R_2 = 220$  is suitable. Then the voltage on the bus with the drivers disconnected and  $U_{CC} = 5\text{ V}$  will be  $2.75\text{ V}$ . During operation, the driver is loaded with the absorbed current in state L and the generated current in state H.

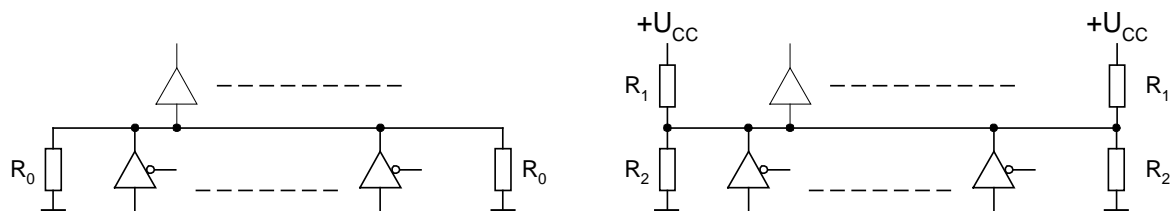


Fig. 26: Terminators with resistors

The disadvantage of the terminator according to Fig. 26 on the right is the large current consumption from the source  $U_{CC}$ . This can be essential for data and address buses with a large number of signals, especially in case of battery-powered systems. Then the solution according to Fig. 27 can be used.

On the left are terminators with an RC combination. Resistor  $R_0$  terminates the line and the capacitor prevents the continuous flow of current through the resistor. The time constant  $R_0 C$  should be selected as at least four times the signal delay time in the line. Resistors  $R_1$  and  $R_2$  have a large value in this case, so that they do not load the voltage source  $U_{CC}$ . Their purpose is not the line termination (this is provided by  $R_0$ ), but to ensure a suitable voltage on the bus when all exciters are disconnected. An undefined voltage usually cannot be accepted.

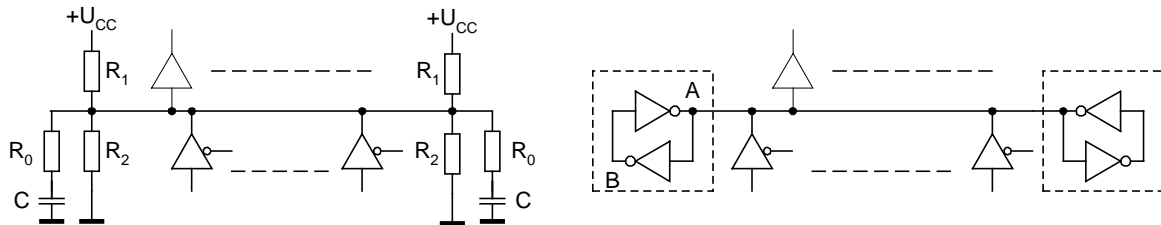


Fig. 27: Low power terminators

Figure 27 on the right shows an **active terminator** ("bus hold"). This is the simplest version of a bistable flip-flop circuit, based on a positive feedback. If  $A = 1$ , then  $B = 0$ , and therefore  $A = 1$ , which is a confirmation of the originally assumed state. The same is true for  $A = 0$  and  $B = 1$ . To toggle the circuit at point A from '1' to '0', state '0' must be forced to point A for a short time, which requires current to be absorbed by one of the bus drivers. Then  $B = 1$ , therefore  $A = 0$  and the current no longer flows. The flip-flop remains in its new state. Similarly, toggling A from '0' to '1' requires supplying current to the point A. This way, the active terminator absorbs the energy of the incoming wave so that it is no longer reflected. At steady state, the active terminator (CMOS) is very economical. A special feature of active terminators is that when all exciters are disconnected, the last state before disconnection remains on the bus.

Input voltage limiters (see Fig. 8) have certain, though not 100%, effect. They prevent voltage surges above  $+U_{CC}$  and below 0 and thus partly suppress reflections.